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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,102	11/19/2003	Kramadhati V. Ravi	42P17822	9900
8791	7590 01/10/2006		EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN 12400 WILSHIRE BOULEVARD SEVENTH FLOOR			PHAM, THANHHA S	
			ART UNIT	PAPER NUMBER
LOS ANGE	ELES, CA 90025-1030	•	2813	
			DATE MAILED: 01/10/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/718,102	RAVI, KRAMADHATI V.				
Office Action Summary	Examiner	Art Unit				
	Thanhha Pham	2813				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period w  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be timulated will expire SIX (6) MONTHS from the cause the application to become ABANDONED	l. ely filed the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on <u>03 N</u>	ovember <u>2005</u> .					
	action is non-final.					
closed in accordance with the practice under E	x parte Quayle, 1935 C.D. 11, 45	3 O.G. 213.				
Disposition of Claims						
4)⊠ Claim(s) <u>1-8 and 22-35</u> is/are pending in the application.						
	4a) Of the above claim(s) <u>2-5, 22, 29-32</u> is/are withdrawn from consideration.					
5) Claim(s) is/are allowed.						
6) Claim(s) 1,6-8,23-28 and 33-35 is/are rejected	· /					
7) Claim(s) is/are objected to.	• • • • • • • • • • • • • • • • • • • •					
8) Claim(s) are subject to restriction and/o	r election requirement.					
Application Papers						
9) The specification is objected to by the Examine	r.					
10) The drawing(s) filed on is/are: a) accepted or b) objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correct						
11)☐ The oath or declaration is objected to by the Ex	caminer. Note the attached Office	Action or form PTO-152.				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a) ☐ All b) ☐ Some * c) ☐ None of:						
1. Certified copies of the priority documents have been received.						
2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau	u (PCT Rule 17.2(a)).					
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) X Notice of References Cited (PTO-892)	4) Interview Summary					
<ul> <li>2) Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)</li> </ul>	Paper No(s)/Mail Da 5) Notice of Informal P	atent Application (PTO-152)				
Paper No(s)/Mail Date <u>2/25/04</u> .	6) Other:					

## **DETAILED ACTION**

This Office Action is in response to Applicant's Election dated 11/03/2005.

#### Election/Restrictions

- 1. Claims 2-5, 22, 29-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species. Applicant timely traversed the restriction (election) requirement in the reply filed on 11/03/2005.
- 2. Applicant's election with traverse of specie D (claims 1, 6-8, 23-28 and 33-35 in the reply filed on 11/03/2005 is acknowledged. The traversal is on the ground(s) that species A-D are not mutually exclusive since independent claims recite a feature that related to a testing a semiconductor tool using a wafer. This is not found persuasive because species A-D (distinct species are cited in dependent claims) are mutually exclusive with reasons given in the Office Action dated 10/18/2005 even though independent claims as generic claims are examined together with elected species. The requirement is still deemed proper and is therefore made FINAL. Examiner also mentions that claim 29 mistakenly included in specie D is also withdrawn from consideration.

## Oath/Declaration

3. Oath/Declaration filed on 11/19/2003 has been acknowledged.

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## Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 6-8, 23-25, 27-28 and 33-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1,

"testing the semiconductor tool using the wafer" renders the claimed indefinite. It is not clear the wafer used for testing the semiconductor tool including the coating or not.

With respect to claim 7,

"a surface of the wafer" renders the claim indefinite. It is not clear that the testing surface contaminant adding properties comprising testing scattering properties of a surface of the wafer (surface of wafer without the coating) or testing scattering properties of a surface of the coating and a surface of which coating is tested.

▶ With respect to claim 23,

it is not clear where a polysilicon layer is provided.

▶ With respect to claim 24,

it is not clear where a polysilicon layer is provided.

With respect to claim 25,

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"removing contaminants from a surface of the coating of the wafer" renders the claim indefinite. The scope of the claim cannot be defined since is not clear that contaminants are removed from a surface of which coating of the wafer – coating in step of providing of claim 1 or coating in step of replacing of claim 1.

With respect to claim 27,

it is not clearly where a polysilicon layer is provided.

With respect to claim 34,

"a surface of the wafer" renders the claimed indefinite. it is not clear that the testing surface contaminant adding properties comprising testing scattering properties of a surface of the wafer (surface of wafer without the coating) or testing scattering properties of a surface of the coating and a surface of which coating is tested.

## Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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6. Claims 1, 6, 8, 25-26, 33 and 35, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Rojihantalab et al [US 6,761,625].

\*\*\* Notice: This rejection is based on the scope of the claim that the wafer, the coating on the wafer before testing the semiconductor tool and the coating on the wafer after replacing step are the same material.

▶ With respect to claim 1, Rojhantalab et al (figs 1-3, cols 1-3) discloses a method comprising:

providing a coating over a wafer (wafer 201 before testing, col 1 lines 8-22: an outer surface of the wafer before testing defining the coating);

testing a semiconductor tool using the coated wafer after the step of providing the coating (col 1 lines 8-22); and

replacing at least a portion of the coating of the wafer with a layer of coating (fig 2-3, col 2 lines 8-63 and col 3 lines 30-45: when the wafer is polished from figs 2-3, the outer surface of the wafer as being mentioned above, outer surface of wafer 201 of fig 2, is removed to expose another fresh coating, outer surface of wafer 301 in figure 3 – thus, at least a portion of the coating of wafer 201 is replaced by a layer of coating, out surface of wafer 301, for testing in subsequent step) wherein each coating comprises at least one characteristic of a single crystal structure.

▶ With respect to claim 26, Rojhantalab et al (figs 1-3, cols 1-3) discloses a method comprising:

replacing at least a portion of a coating of a wafer with a layer of a coating of a wafer with a layer of coating (fig 2-3, col 2 lines 8-63 and col 3 lines 30-45: when the wafer is polished from figs 2-3, the outer surface of the wafer as being mentioned above, outer surface of wafer 201 of fig 2, is removed to expose another fresh coating, outer surface of wafer 301 in figure 3 –

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thus, at least a portion of the coating of wafer 201 is replaced by a layer of coating of out surface of wafer 301 for testing in subsequent step) wherein each coating has at least one characteristic of a single crystal structure (col 2 lines 34-38); and

testing at least on characteristics of a semiconductor tool using the coated wafer (col 1 lines 8-31).

- ▶ With respect to claims 6 and 33, Rojhantalab et al (col 1 lines 8-31) discloses testing surface contaminant adding properties of the semiconductor tool.
- ▶ With respect to claim 25, Rojhantalab et al (figs 2-3) discloses removing contaminants from a surface of the coating of wafer in the step of providing after the testing the semiconductor tool.
- ► With respect to claims 8 and 35, at least one characteristic of the single crystal structure (single silicon crystal) comprises insignificant distortion of an angle of refraction of incident light.

## Claim Rejections - 35 USC § 103

- 7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
  - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 8. Claims 7 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rojhantalab et al [US 5,761,625] in view of Steigneier et al [US 4,526,468].

Rojhantalab et al substantially discloses the claimed method including testing the semiconductor to by checking defects on wafer. Rojhantalab et al does not testing light scattering properties on the coated wafer including coating comprising at least one characteristic of a single crystal structure.

However, Steigneier et al teaches testing light scattering properties on the coated wafer comprising the single crystal structure to detect defect/contaminants of the coated wafer.

Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Rojhantalab et al by testing light scattering properties on the coated wafer to defect defects/contaminants, as taught by Steigneier, to test surface contaminant adding properties caused by semiconductor tool.

#### Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thanhha Pham